Remarks

Concerning Item 2 of the subject action, the Examiner rejects claims 1-3, 5, and 7-11, under 35 USC §103(a) based on the combination of the teachings of Neisch et al (U.S. Patent No.: 6,269,319; hereinafter Neisch) and Zwan et al (U.S. Patent No.: 6,098,028; hereinafter Zwan).

Concerning claim 1, the applicant claims:

> A method of sequentially connecting one or more testing devices to I/O ports of a DUT through a switching network, so as to execute a predetermined testing procedure associated with the DUT, comprising: (a) generating a switching network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the switching network to an output of the switching network, wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT; (b) receiving one or more commands, wherein each of the commands uniquely specifies an electrical path connecting a particular testing device to a particular I/O port of the DUT; and, (c) for each of the one or more commands, comparing the command to the switching network map so as to identify a corresponding electrical path through the switching network, and implementing the corresponding electrical path associated with the command through the switching network; and, (d) sequentially implementing the electrical paths corresponding to the one or more commands in a predetermined order.

Applicant respectfully asserts that the combination of the teachings of Neisch and Zwan fails to disclose elements (a) and (c) of applicant's claim 1 and, therefore, is not a proper basis for a 35 USC §103(a) rejection, as the combination fails to disclose each and every element of the applicant's claimed invention.

Concerning element (a) of applicant's claim 1, namely "generating a ***switching network map*** defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the switching network to an output of the switching network, wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT", the Examiner relies on various portions of Zwan to disclose the generation and use of a switching network map, namely column 5, lines 21-36, column 5, lines 10-20, and column 7, line 47 – column 8, line 8.

As will be discussed below in greater detail, the applicant respectfully asserts that the referenced portions of Zwan neither teach nor disclose elements (a) and (c) of applicant's claim 1, alone or in combination with the teachings of Neisch.

Concerning column 5, lines 10-20, this passage discloses:

> Switch matrix 200 allows for a completely non-blocking arrangement of communications pathways between each of the elements of the test device 20. Switch matrix 200 provides switching for data as well as clock signals through the switch fabric and maintains suitable clock and data relationships. Switch 200 cross connects DS1 signals from the M13 mux 100, SONET module 40, ATM Processor 90, DS1 line interface 140 and DS1 processor 142. Similarly, switch 200 cross-connects DS3 signals from M13 mux 100, SONET module 40, ATM processor 90, DS3 line interface 110 and DS3 processor 112. These communications pathways are thus selectable as desired.

The above-listed passage concerns the manner in which switch matrix 200 allows for the routing of signals between various elements of the test device disclosed in Zwan. Various examples are provided that demonstrate the manner in which switch matrix 200 may interconnect various components. However, the applicant respectfully reminds the examiner that the applicant's claim 1 is not merely directed toward a switching network, but uniquely concerns the manner in which a switching network map is used to configure a switching network.

Concerning column 5, lines 21-36, this passage discloses:

> Switch 200 allows the following connections in a non-blocking manner for DS1 signals:

1)	To SONET Module 40		
		From:	DS1 Line Interface 140
			DS1 Processor 142
2)	To Mi13 Mux 100		
		From:	DS1 Line Interface 140
			DS1 Processor 142
3)	To ATM Processor 90		
		From:	DS1 Line Interface 140
			DS1 Processor 142
4)	To DS1 Line Interface 140	From:	M13 Mux 100
			SONET Module 40
			ATM Processor 90
			DS1 Processor 142
5)	To DS1 Processor 142		
		From:	M13 Mux 100
			SONET Module 40

ATM Processor 90
DS1 Line Interface 140

It appears that this passage lies at the root of the examiner's assertion that Zwan discloses the use of a switching network map, as the applicant seems to equate the above-listed table to that of the applicant's switching network map. For the reasons discussed below, the applicant respectfully asserts that the examiner's reliance upon this passage is unfounded.

Specifically, this above-listed passage merely is included in the specification of Zwan to provide examples of the various ways in which "switch 200" of Zwan allows for the interconnection of various components of the Zwan system. For example, entry 1 in the above listed table discloses to the reader of the Zwan patent that "switch 200" allows for the interconnection of "SONET Module 40" and "DS1 Line Interface 140" or "DS1 Processor 142". Accordingly, the above-listed table relied upon by the examiner does not provide any insight concerning internal navigation within "switch 200" of Zwan, as Zwan treats "switch 200" as a black box (i.e., a box who's contents are unknown). Therefore, the above-listed table does not disclose the manner in which individual devices (e.g., switches, relays, or conductive paths, for example) within "switch 200" need to be set in order to facilitate the interconnection of, e.g., "SONET Module 40" and "DS1 Line Interface 140", as it merely discloses the end result and not the manner in which that result is achieved.

TO (POGO PIN)	CONN NAME	DEF	FROM (TESTER)	CONNECT	DISCONNECT	COMMENT
S_SMS1	F_10 MHZ	X	SMS1	+K1	-K1	10 MHZ FILTER ON SMS 1
	F_100 MHZ		SMS1	+K2	-K2	100 MHZ FILTER ON SMS 1
	AP	X	AP1	+K3	-K3	AP CONNECTION TO S_SMS 1
S_SMS2	F_10 MHZ	X	SMS2	+K4	-K4	
	F_100 MHZ		SMS2	+K5	-K5	
	AP	X	AP2	+K6	-K6	
S_SMS3	F_10 MHZ	X	SMS3	+K7	-K7	
	F_100 MHZ		SMS3	+K8	-K8	
	AP	X	AP3	+K9	-K9	
S_SMS4	F_10 MHZ	X	SMS4	+K10	-K10	
	F_100 MHZ		SMS4	+K11	-K11	
	AP	X	AP4	+K12	-K12	
S_RF1			RF1			
S_RF2			RF2			

140

FIG. 4

Conversely, as clearly shown in applicant's FIG. 4 (embedded @ right), the applicant's switching network map 140 provides component level instructions that allow for the desired mapping of electrical signals through a switching network. Concerning switching network map 140, the applicant's specification discloses:

> An exemplary SCM map 140, associated with the SCM 104 of FIG. 3, is shown in FIG. 4. The "To" column defines the name of the pogo pin available to the DUT board 106. The "Conn Name" column defines the name given to the specific connection from the pogo pin back to the tester resource. This name can be left out if there is only one connection (as is the case for the RF pins in this example). Note that the connection names are not unique across different pogo pins. This allows them to be easily used in multi-site applications. Internally, the "To" name is used to make each connection name unique. The "From" column defines the tester resource 102 that is used for a particular connection. In some embodiments, a popup menu of possible tester resources could be available to a user to specify the resources in this column. The "Connect" column defines the activities that need to occur in order for the specified connection to be made. In the exemplary system of FIG. 3, all of the connections are made by throwing a single relay, e.g., the AP connection of S_SMS1 is established by closing the K3 relay. The "Disconnect" column defines the activities that need to occur in order for the specified connection to be disconnected, and has the same format as does the "Connect" column. The "Def" column is a checkbox that indicates which of the SCM connections are exported to the DUT board by default. Connections which are not checked must be explicitly specified by the user in order to be available.

As disclosed above, switching network map 140 provides specific component-level instructions (e.g., the AP connection of S_SMS1 is established by closing the K3 relay) that, when implemented, allow for the desired mapping of electrical signals through a switching network. Accordingly, the applicant's switching network map is clearly distinguishable from the above-listed table disclosed in Zwan at column 5, lines 21-36.

Further, what must be realized is that the applicant's claimed invention compares received commands to the switching network map "to identify a corresponding electrical path through the switching network" (i.e., element C of applicant's claim 1). However, the above-referenced table disclosed in Zwan at column 5, lines 21-36 merely demonstrates the various ways in which switch 200 may interconnect components. Specifically, the above-referenced table is neither disclosed nor taught to be a machine-readable table that is used to automatically configure a switching network. Accordingly, the Zwan system never compares received commands to the above-referenced table "to identify a corresponding electrical path through the switching network", as claimed by element C of applicant's claim 1.

Concerning column 7, line 47 – column 8, line 8, this passage discloses:

> A further example is set forth in FIG. 7. In FIG. 7, the function of an external network element such as a SONET mux must be analyzed to determine whether its SONET mapping functions are sound. In order to test this function, it is desired to produce a DS1 signal, embed that signal within a SONET OC-12 signal, and have the external SONET mux demap that signal into its constituent signals and return the original DS1 test signal for evaluation by the test device. In order to configure the switch to accomplish this test, the user would first select the DS1 pad 172 to indicate DS1 mapping. The user would then select the output of DS1 processor representation 158 and then the input to SONET module representation 152. The system would then show a dashed connection between element 158 and 152. By selecting "confirm" that connection becomes solid indicating that the system has accepted that configuration. Next, the user would select the input of the DS1 processor 158 and the output of the DS1 line interface 156, press confirm. User then would exit the switch matrix and choose the DS1 test set, and set the desired transmit parameters and form of the results for display on selective display 50. In this manner, a complex test protocol is implemented in a fully intuitive and natural manner. The key to this ease of implementation is the graphical representation of switch matrix 202 and the related system elements. By providing the user with the ability to see and point to desired signal paths, little or no training is required to operate the system. This results in significant savings to those engaged in the operation and maintenance of communications network elements.

The above-referenced passage further reinforces the argument made by the applicant concerning the failure of Zwan (alone or in combination with the teachings of Neisch) to disclose "a switching network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the switching network to an output of the switching network".

Specifically, the above-referenced passage describes a typical testing procedure employed by a user to test a component. This passages discloses that "the user would first select the DS1 pad 172 to indicate DS1 mapping", "[t]he user would then select the output of DS1 processor representation 158 and then the input to SONET module representation 152", and "the user would select the input of the DS1 processor 158 and the output of the DS1 line interface 156". Once the users has completed selection of the appropriate inputs and outputs, the user would "press confirm". Accordingly, when using the Zwan system, the user must manually configure the system and then confirm the configuration. Therefore, Zwan does not teach a

system that compares received commands to the switching network map "to identify a corresponding electrical path through the switching network".

For the above-stated reasons, the applicant respectfully asserts that the combination of the teachings of Neisch and Zwan fails to disclose elements (a) and (c) of applicant's claim 1 and, therefore, is not a proper basis for a 35 USC §103(a) rejection, as the combination fails to disclose each and every element of the applicant's claimed invention.

Accordingly, the applicant respectfully asserts that applicant's claim 1 is patentable over the combination of the cited references. Further, as claim 2-7 all depend (either directly or indirectly) upon claim 1, the applicant respectfully asserts that these claims are also patentable.

Concerning claim 8, the applicant claims:

> A system for sequentially connecting one or more testing devices to I/O ports of a DUT through a switching network, so as to execute a predetermined testing procedure associated with the DUT, comprising: (a) a switching network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the switching network to an output of the switching network, wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT; (b) a controller for (i) receiving one or more commands, wherein each of the commands uniquely specifies an electrical path connecting a particular testing device to a particular I/O port of the DUT, (ii) comparing each of the commands to the switching network map so as to identify a corresponding electrical path through the switching network, and implementing the corresponding electrical path associated with the command through the switching network, and (iii) sequentially implementing the electrical paths corresponding to the one or more commands in a predetermined order.

For the reasons discussed above, the applicant respectfully asserts that the combination of the teachings of Neisch and Zwan fails to disclose elements (a) and (b) of applicant's claim 8 and, therefore, is not a proper basis for a 35 USC §103(a) rejection, as the combination fails to disclose each and every element of the applicant's claimed invention.

Accordingly, the applicant respectfully asserts that applicant's claim 8 is patentable over the combination of the cited references. Further, as claims 9-11 all depend (either directly or indirectly) upon claim 8, the applicant respectfully asserts that these claims are also patentable.

Concerning Item 3 of the subject action, the examiner rejects claim 4, under 35 USC §103(a), based on the combination of the teachings of Neisch, Zwan, and Yang (U.S. Patent No.: 6,098,027).

The applicant respectfully asserts that claim 4 is patentable over the cited combination of references as it depends upon claim 1, which the applicant respectfully asserts (for the reasons discussed above) is a patentable base claim.

Concerning Item 4 of the subject action, the examiner rejects claim 6, under 35 USC §103(a), based on the combination of the teachings of Neisch, Zwan, and Mogi et al (U.S. Patent No.: 4,810,958).

The applicant respectfully asserts that claim 6 is patentable over the cited references as it depends upon claim 1, which the applicant respectfully asserts (for the reasons discussed above) is a patentable base claim.

In closing, the applicant respectfully asserts that the subject application is now in condition for allowance. Please apply any charges or credits to deposit account 50-1133.

Respectfully submitted,

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